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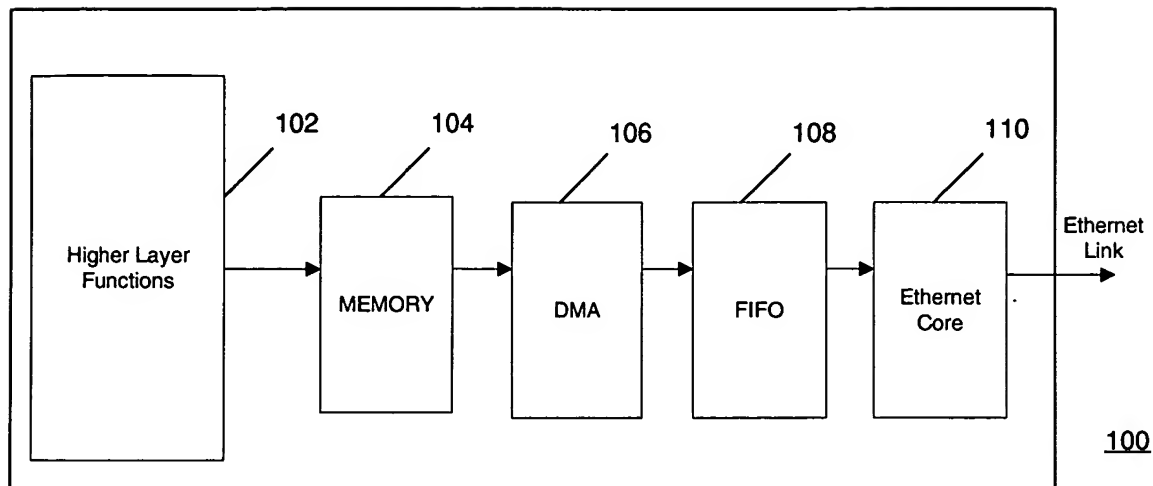


FIG. 1

	Byte Lane 0	Byte Lane 1	Byte Lane 2	Byte Lane 3	Byte Lane 4	Byte Lane 5	Byte Lane 6	Byte Lane 7
X00h	x	x	x	0	1	2	3	4
X08h	5	6	7	8	9	10	11	12
X10h	13	14	15	16	17	18	19	20
X18h	21	22	23	24	25	26	27	28
X18h	29	30	31	x	x	x	x	x

FIG. 2

	Byte Lane 0	Byte Lane 1	Byte Lane 2	Byte Lane 3	Byte Lane 4	Byte Lane 5	Byte Lane 6	Byte Lane 7
X00h	0	1	2	3	4	5	6	7
X08h	8	9	10	11	12	13	14	15
X10h	16	17	18	19	20	21	22	23
X18h	24	25	26	27	28	29	30	31

FIG. 3

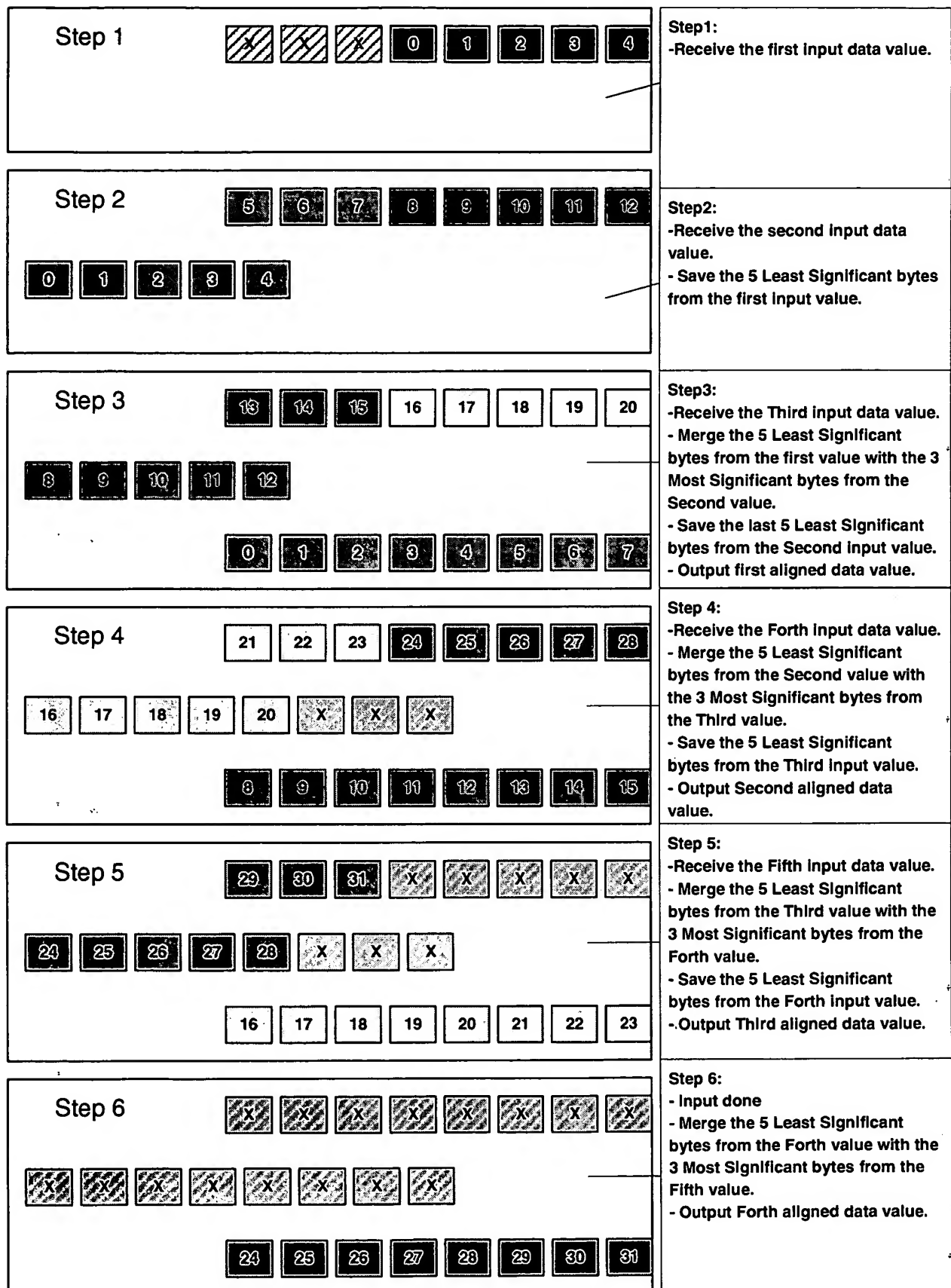


FIG. 4

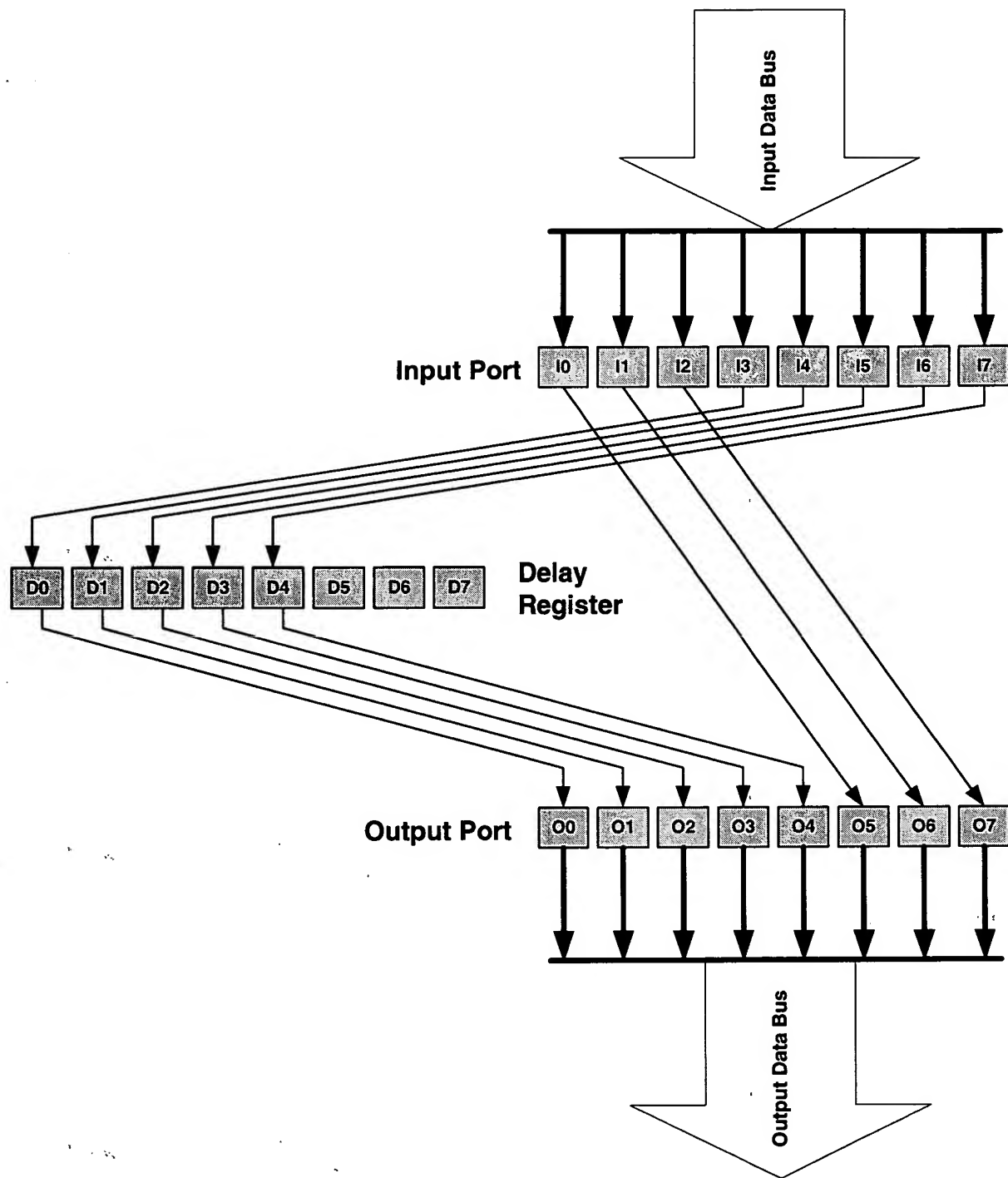


FIG. 5

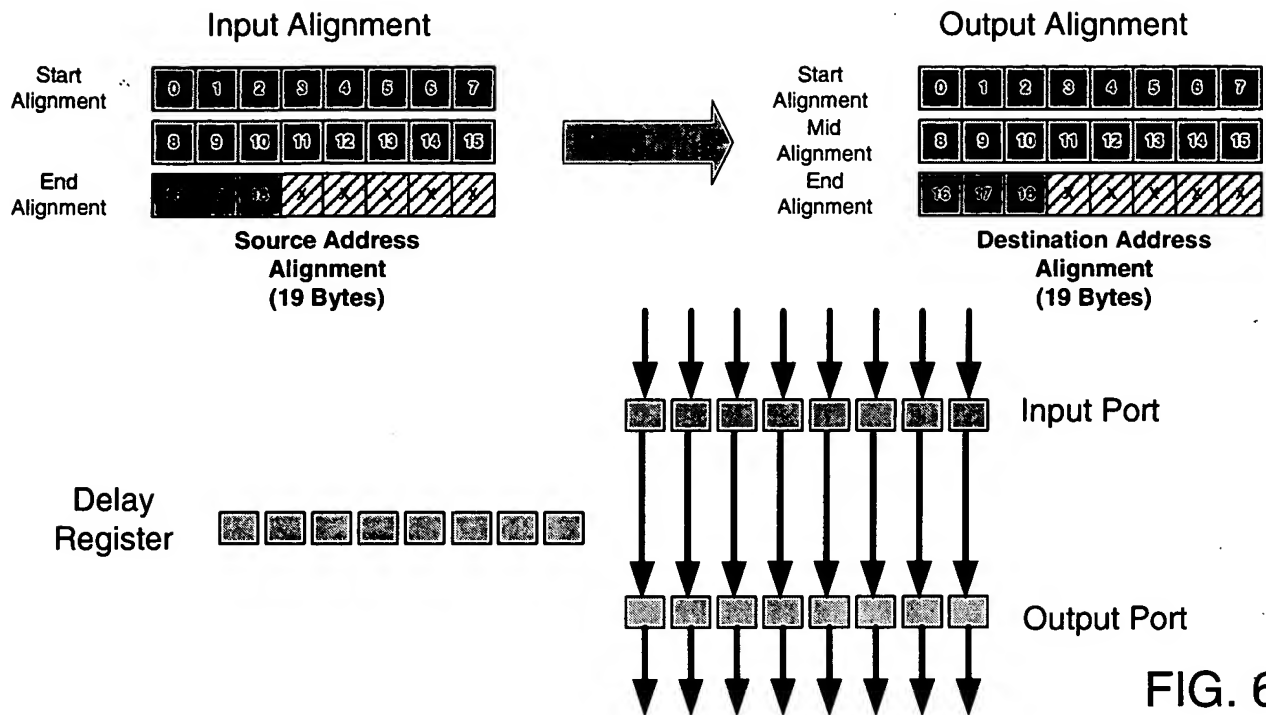


FIG. 6

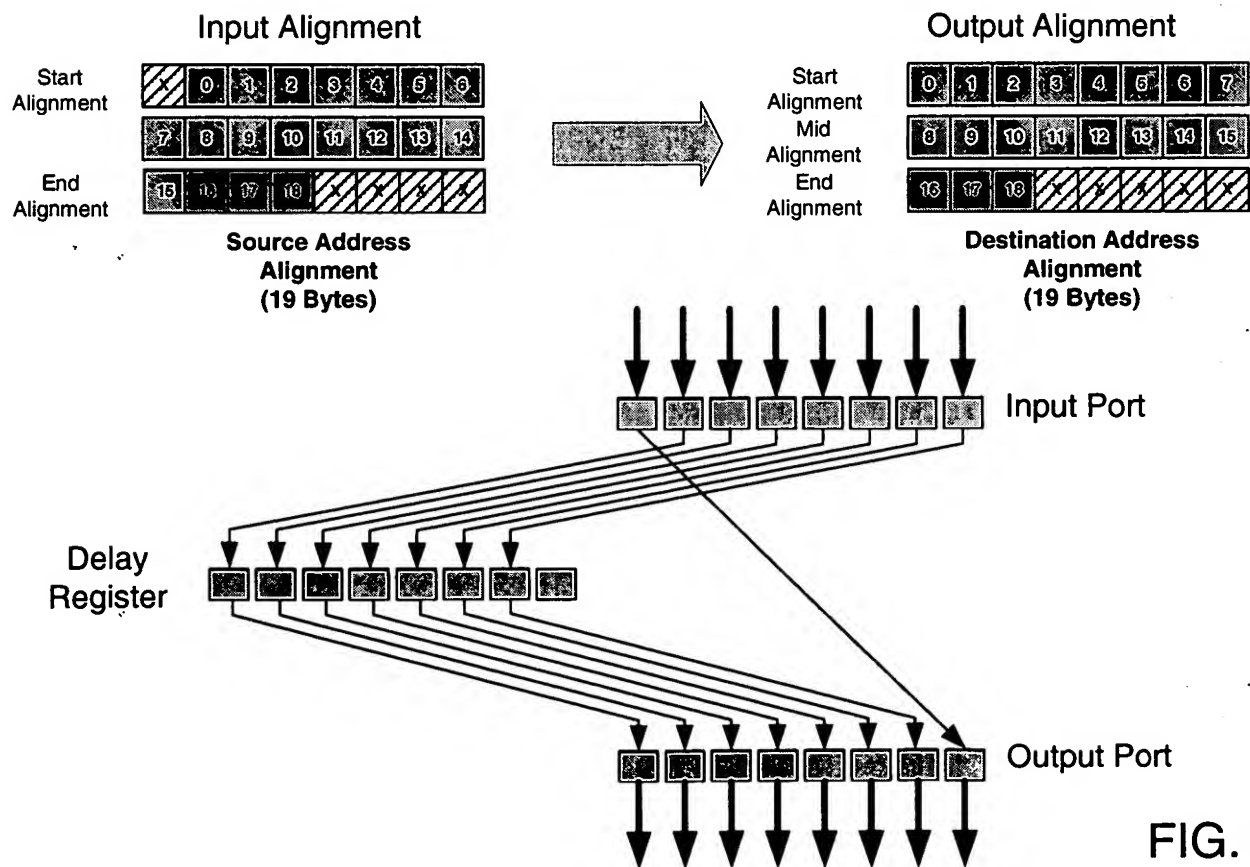
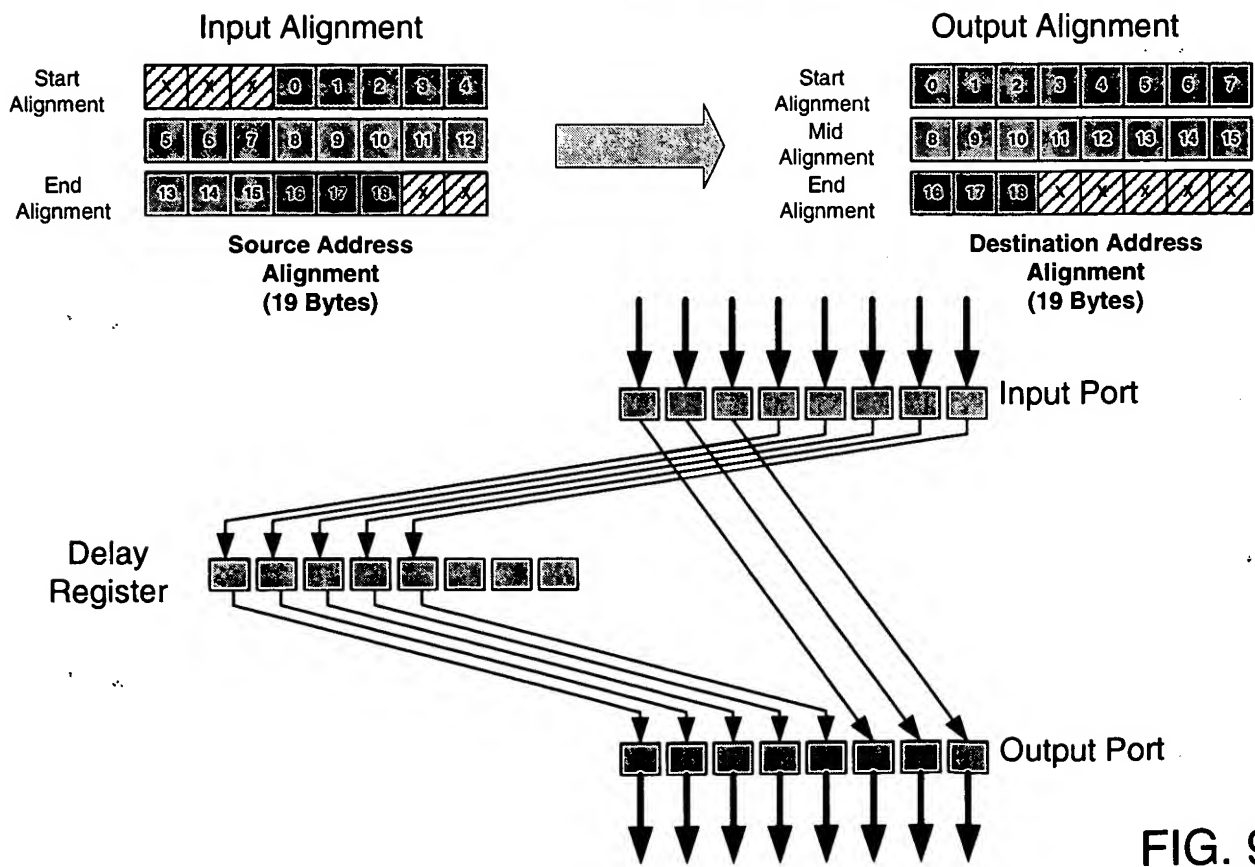
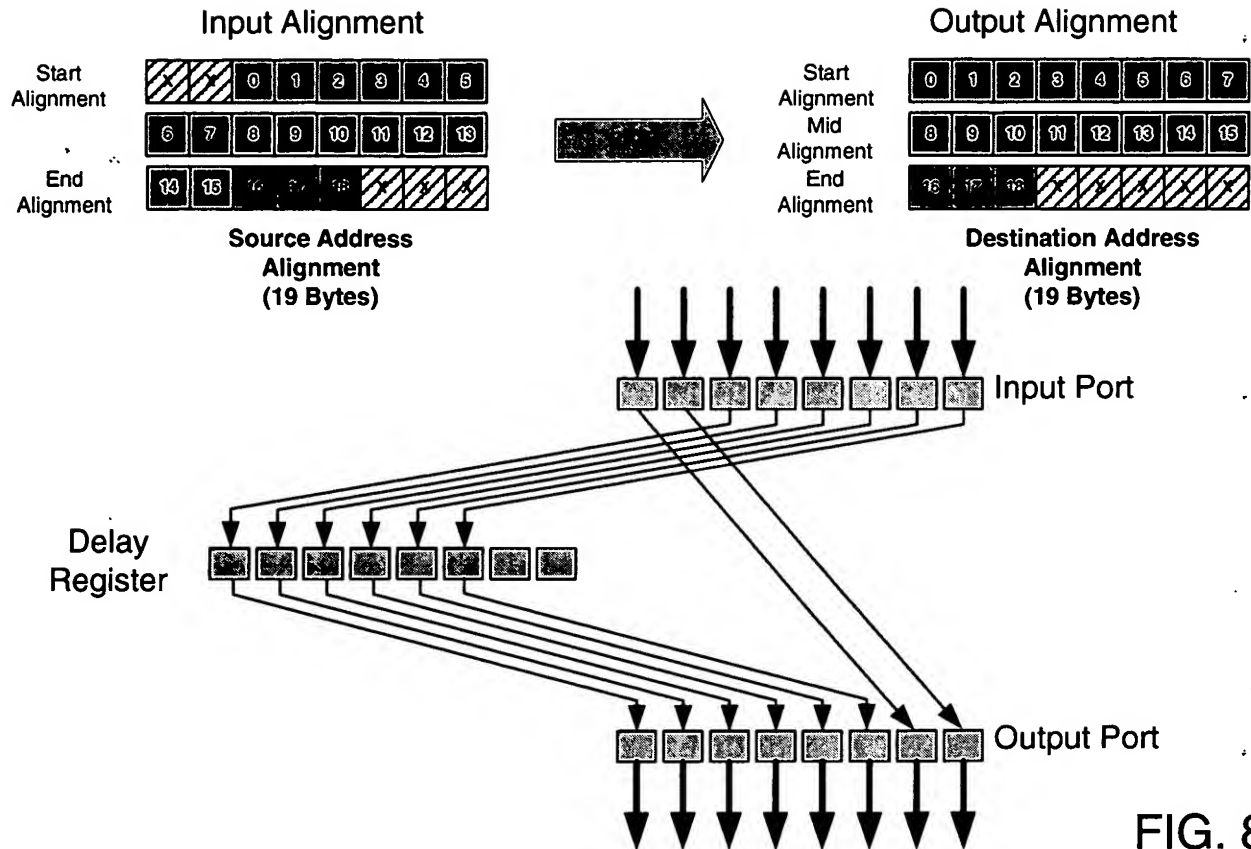


FIG. 7



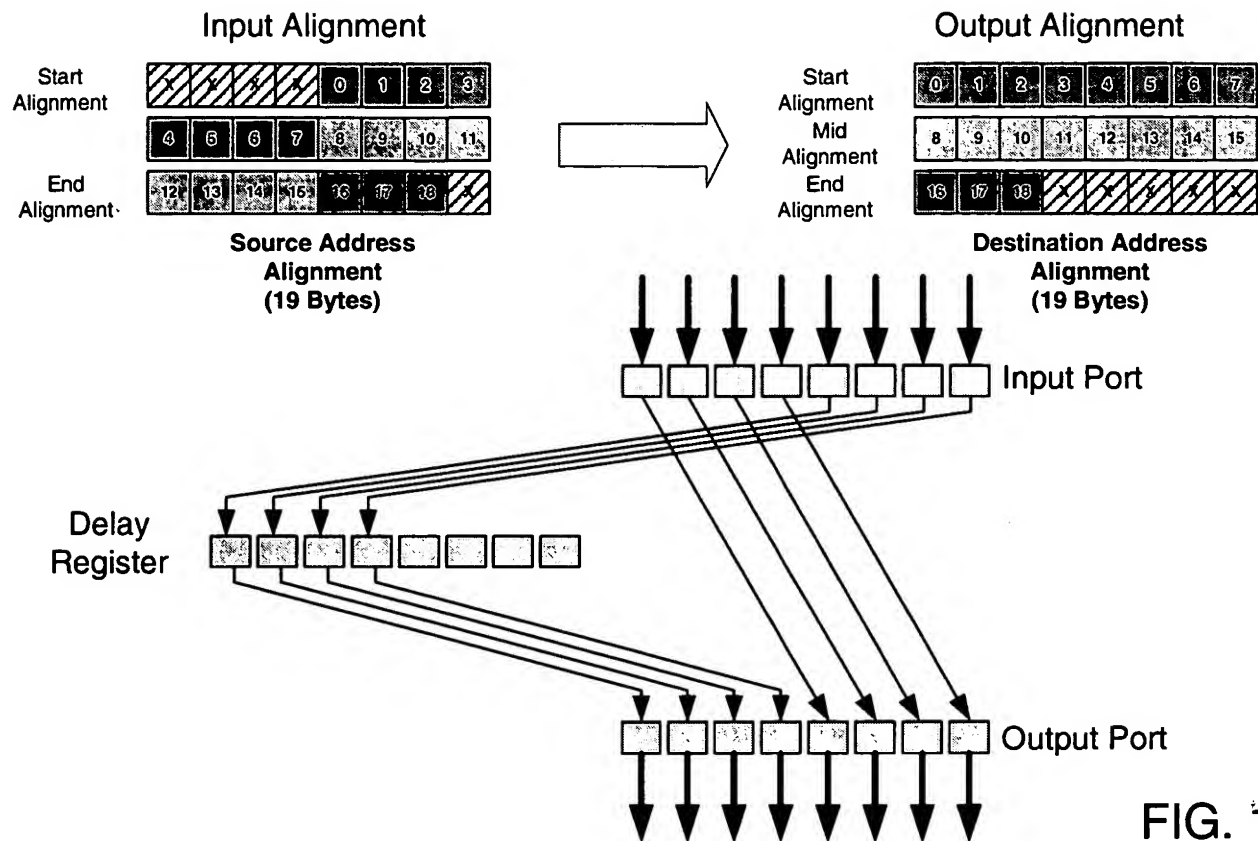


FIG. 10

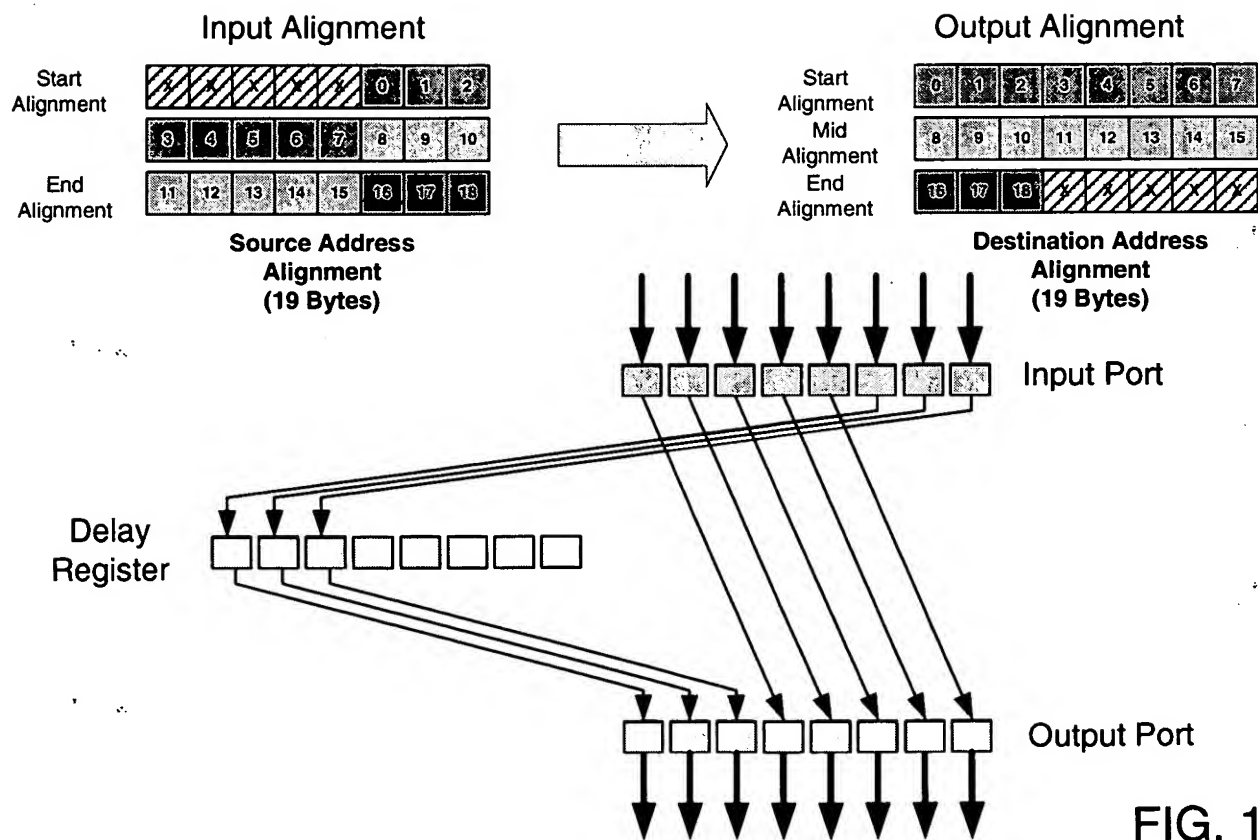


FIG. 11

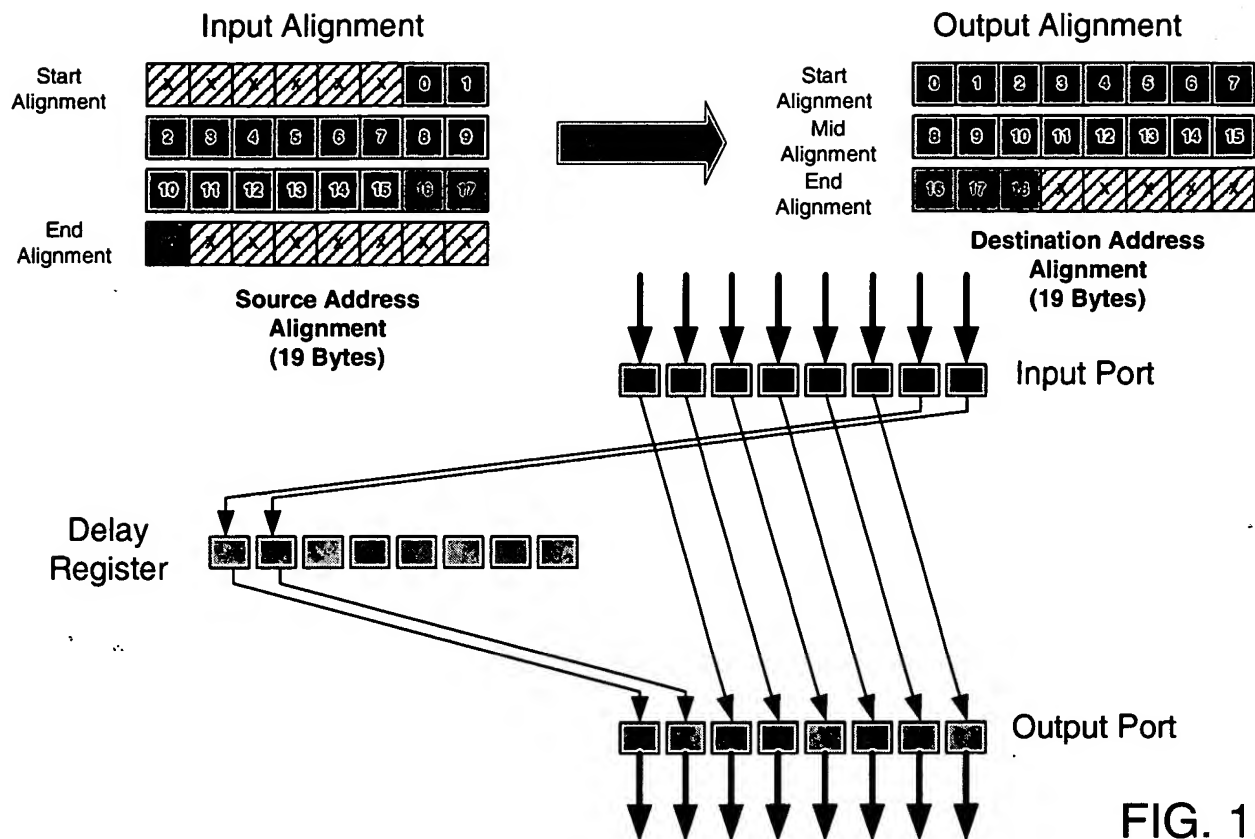


FIG. 12

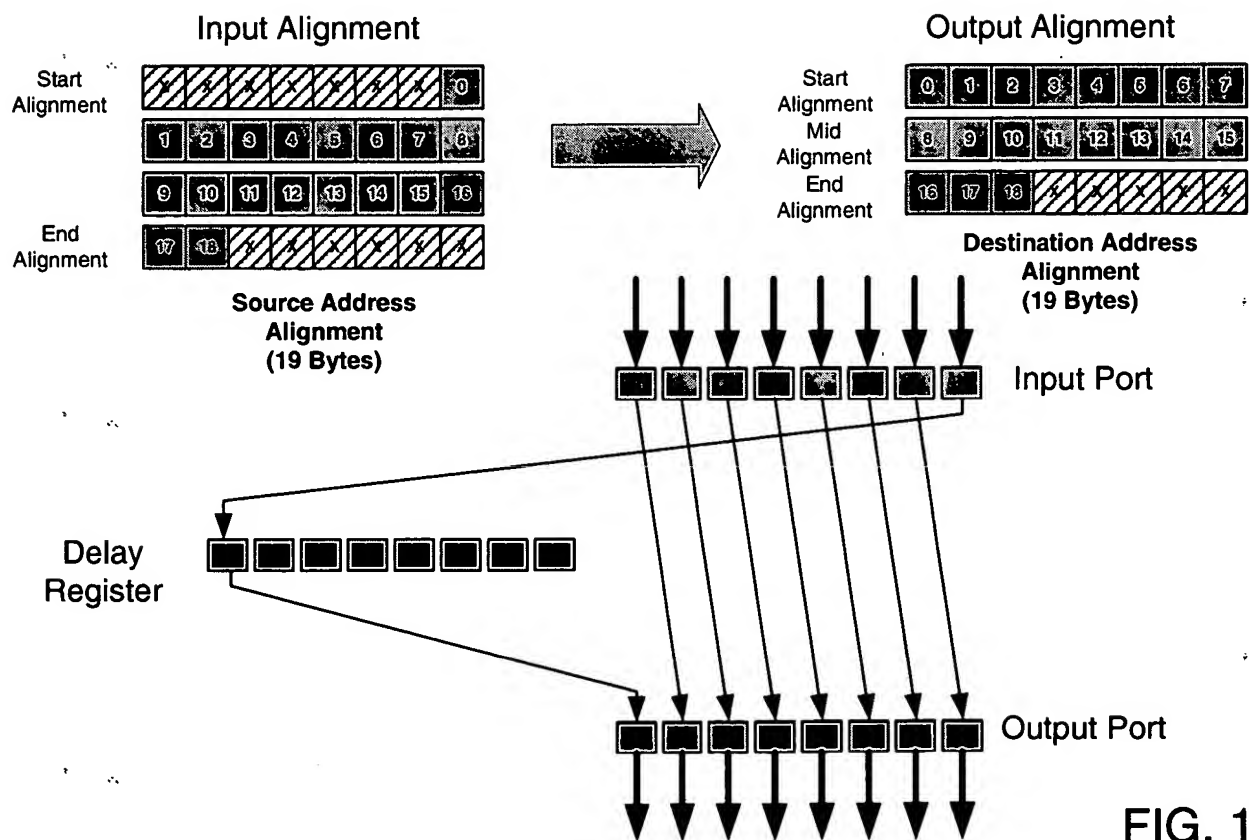


FIG. 13

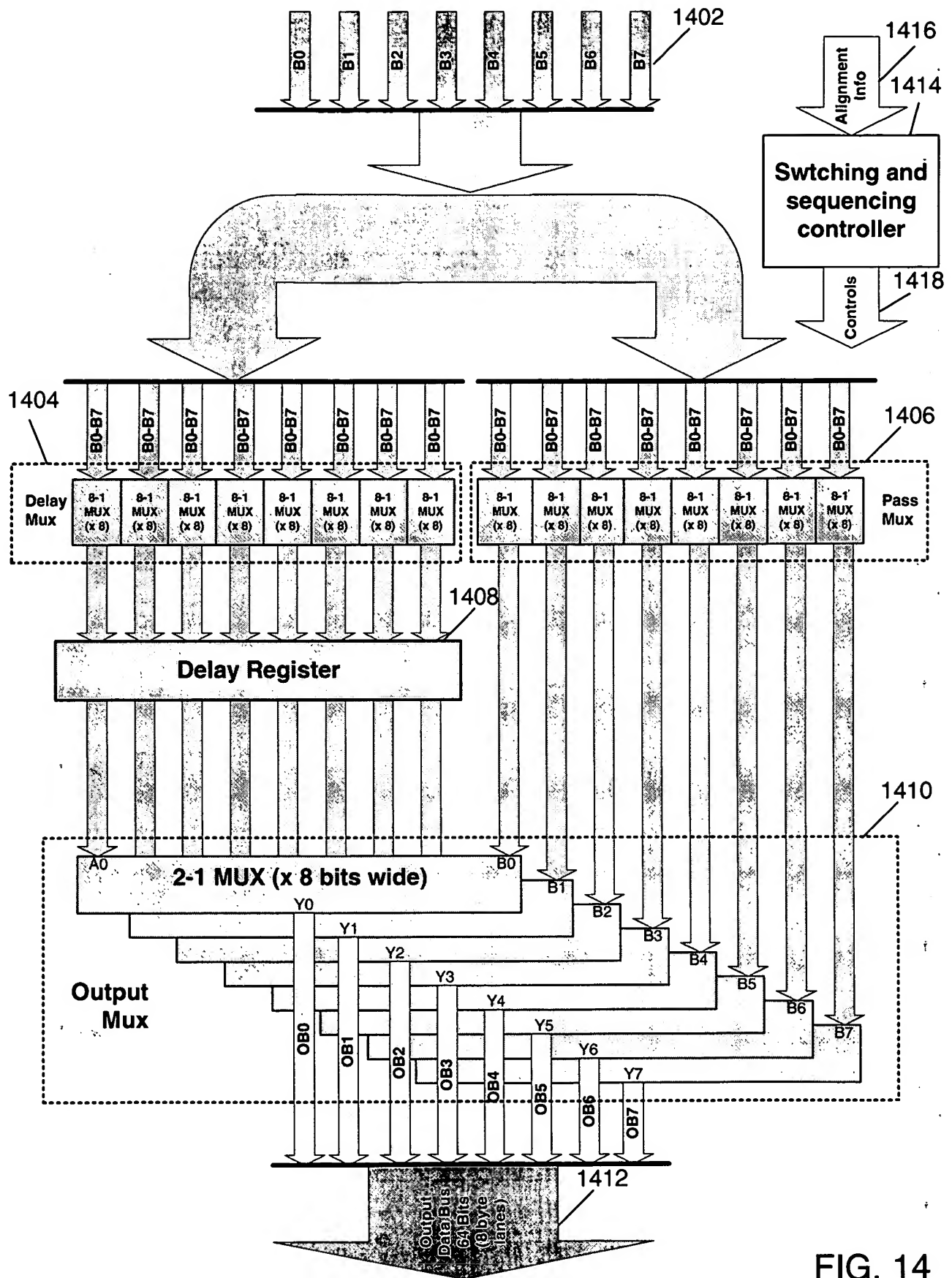


FIG. 14

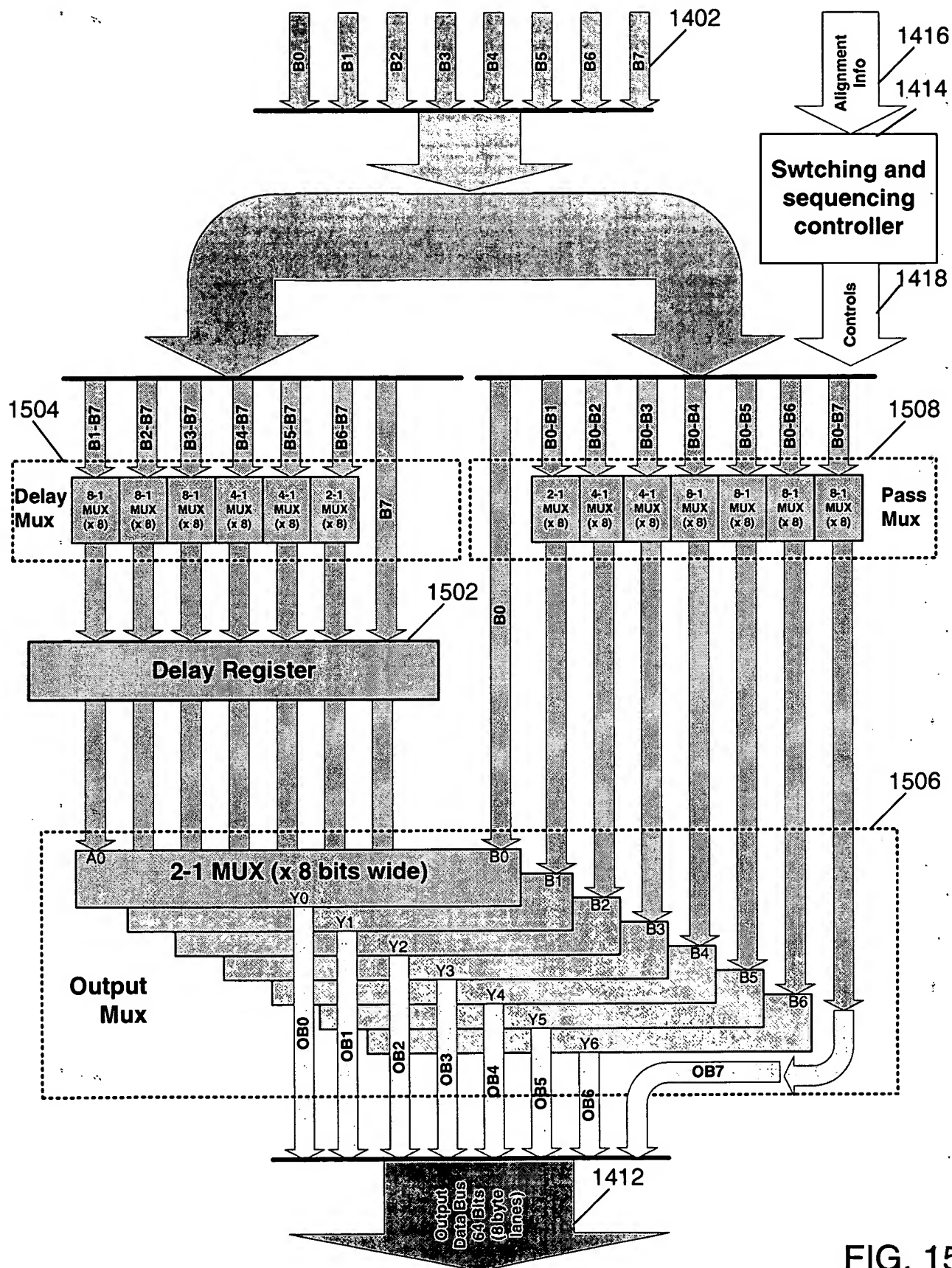


FIG. 15

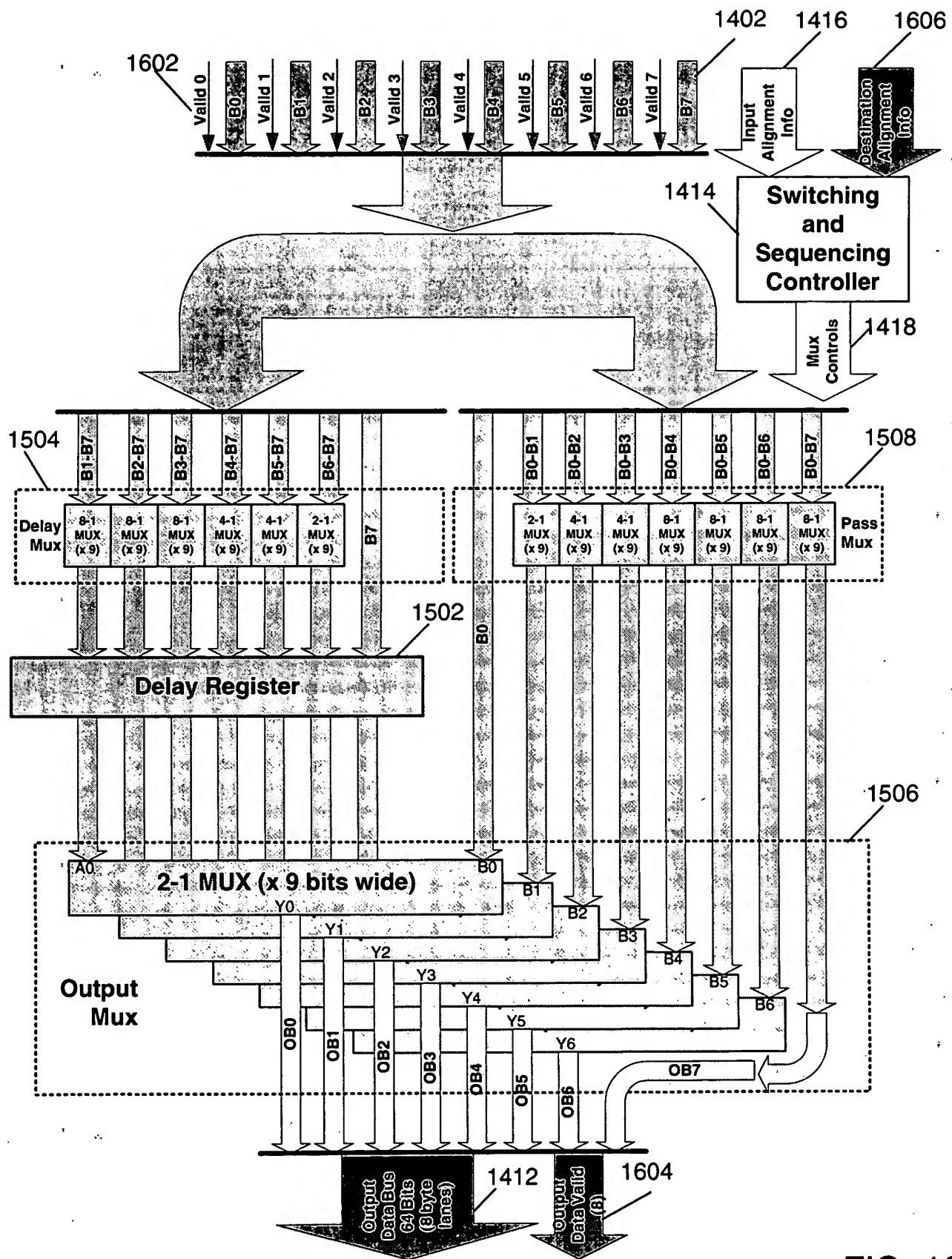


FIG. 16

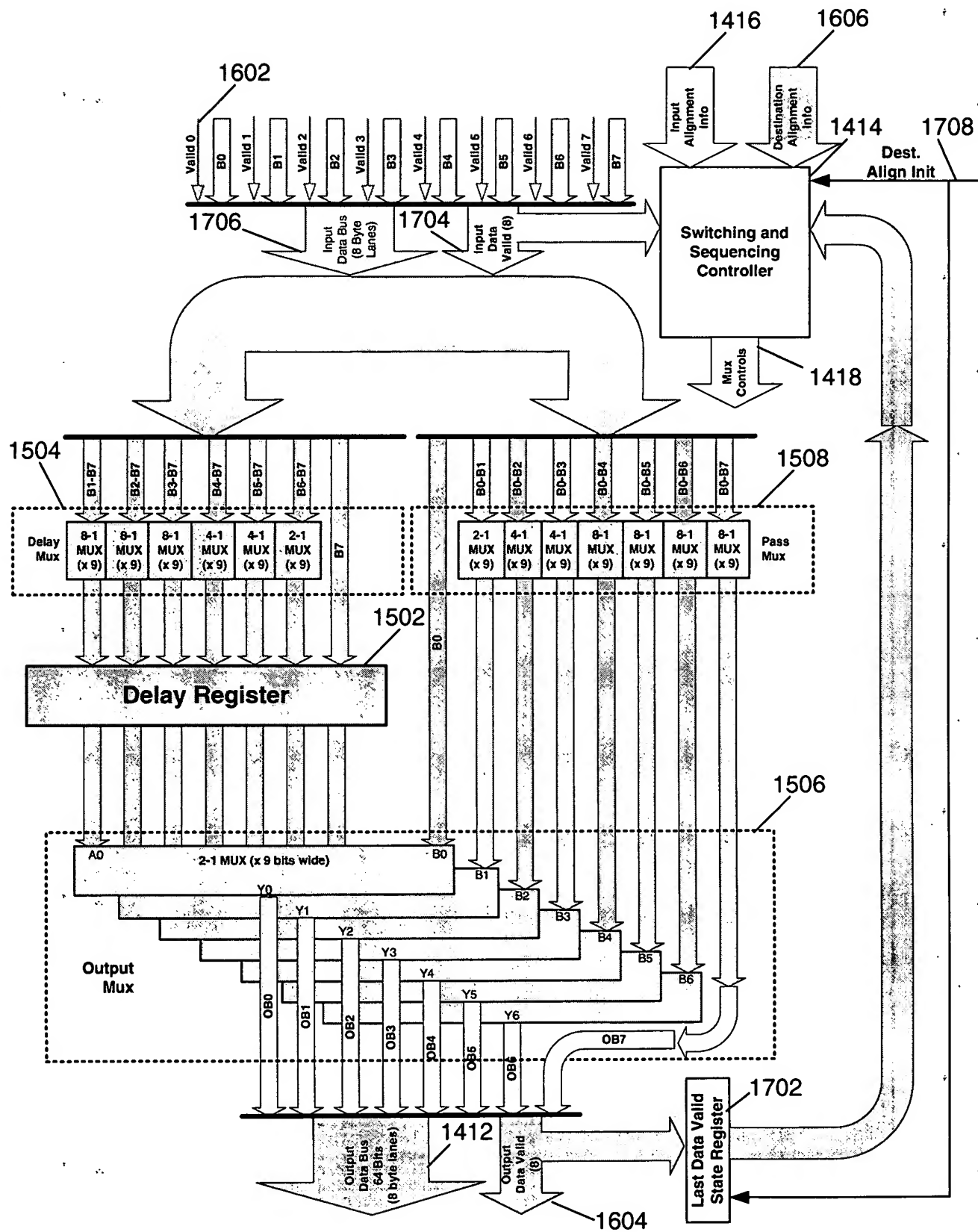


FIG. 17

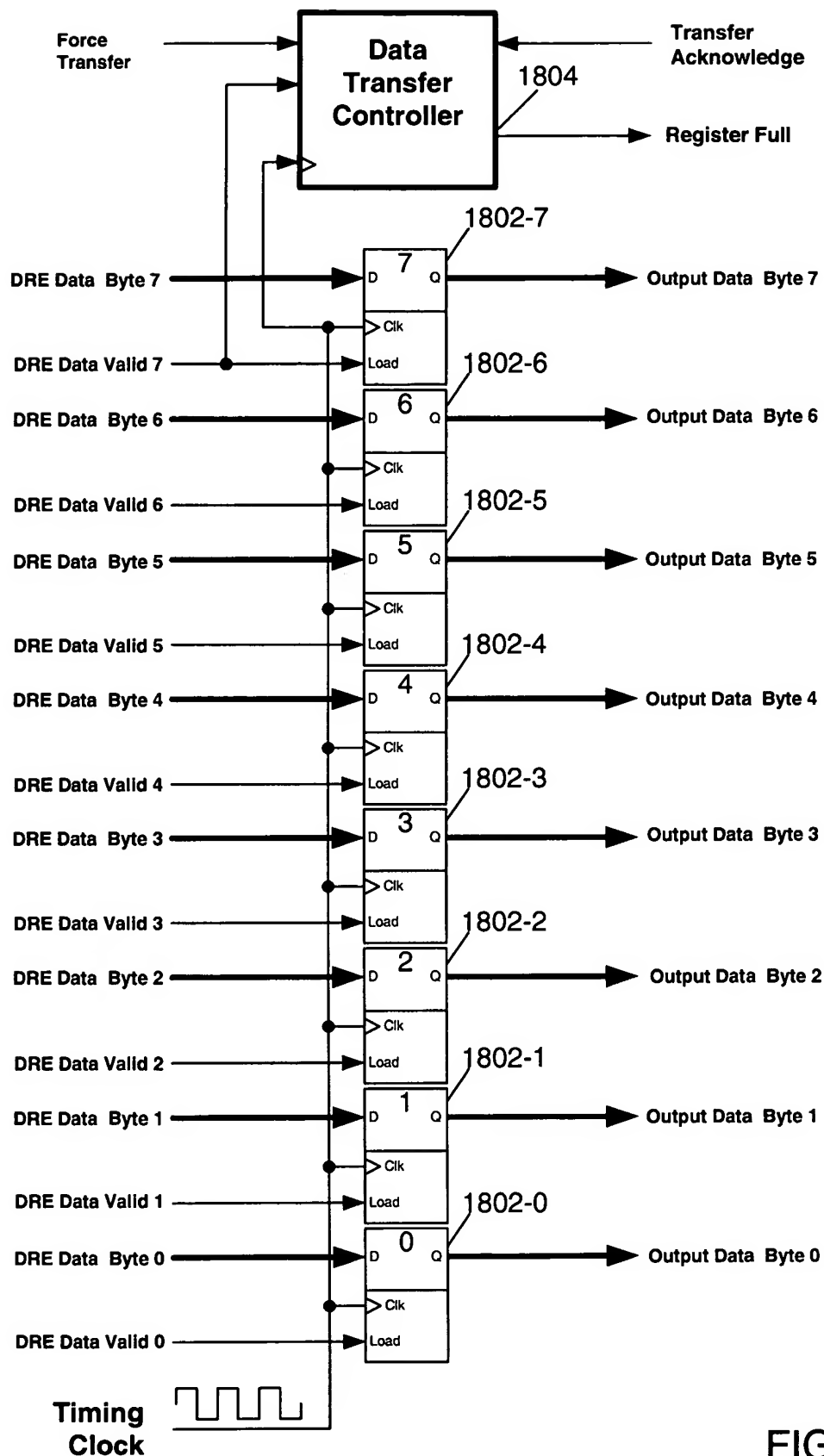


FIG. 18

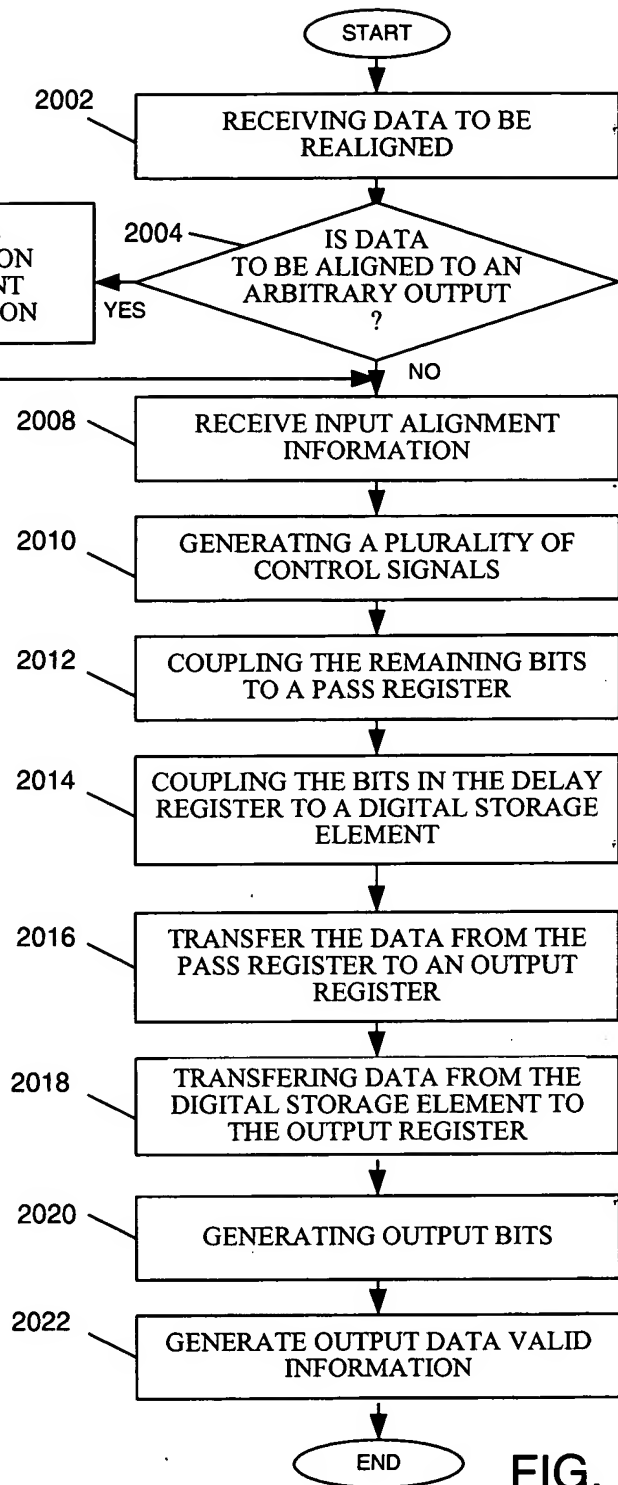
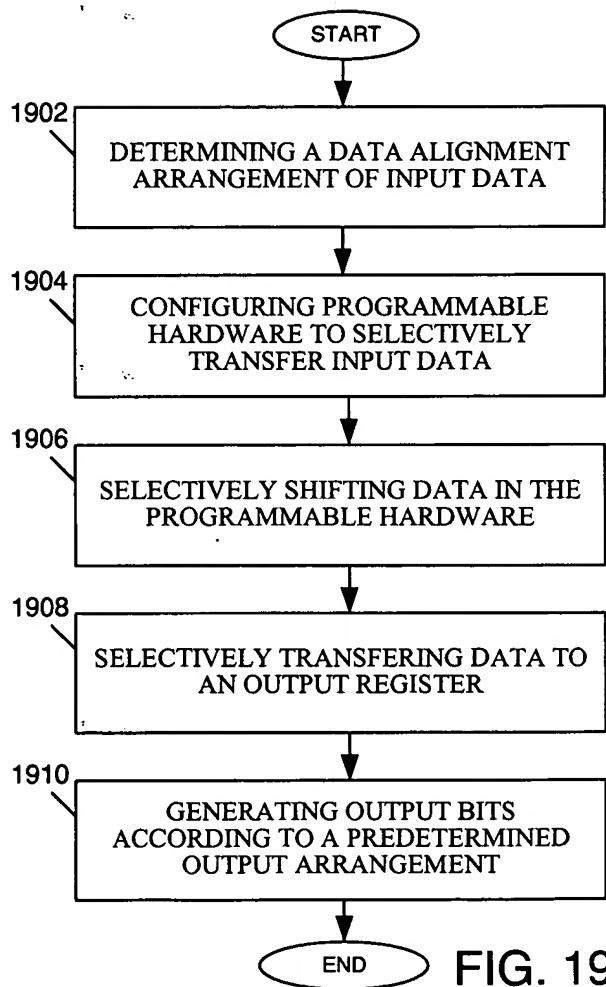


FIG. 20

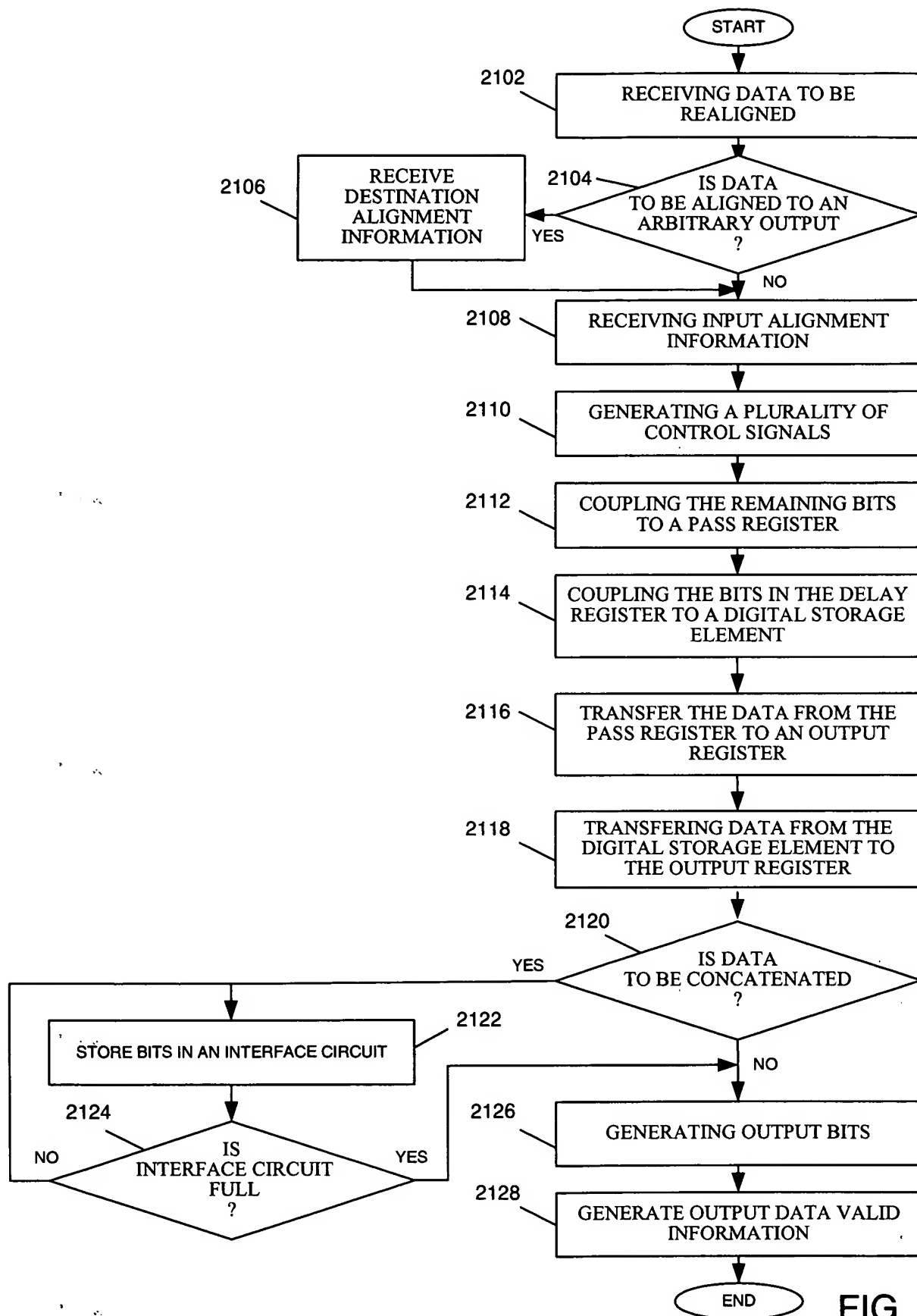


FIG. 21